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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,843	07/21/2003	Veronika Polei	P2002,0618	6526

24131 7590 12/23/2004

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,843	POLEI ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Drawings

The drawings are objected to because in FIG. 3, the drawing should demonstrate that the spacers 12 are being formed in the trench before the poly-silicon layer 11 is deposited therein. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended. " If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
(f) he did not himself invent the subject matter sought to be patented.

Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated by Palm et al. (U.S. Patent 6,548,861).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 1, **Palm** discloses a method for fabricating a buried bit line for a semiconductor memory, which comprises: producing strip-like doped regions parallel to and at distances from one another in a semiconductor body **1**, the regions being adapted to act as bit lines and as source/drain regions **(3, 4)** of a respective memory transistor (col. 5, line 47 to col. 6, line 19 and FIGS. 2b and 3);

FIG 2b

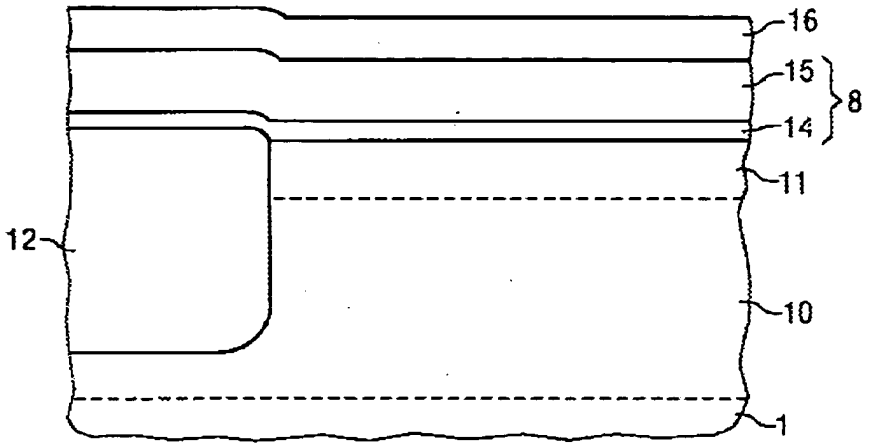
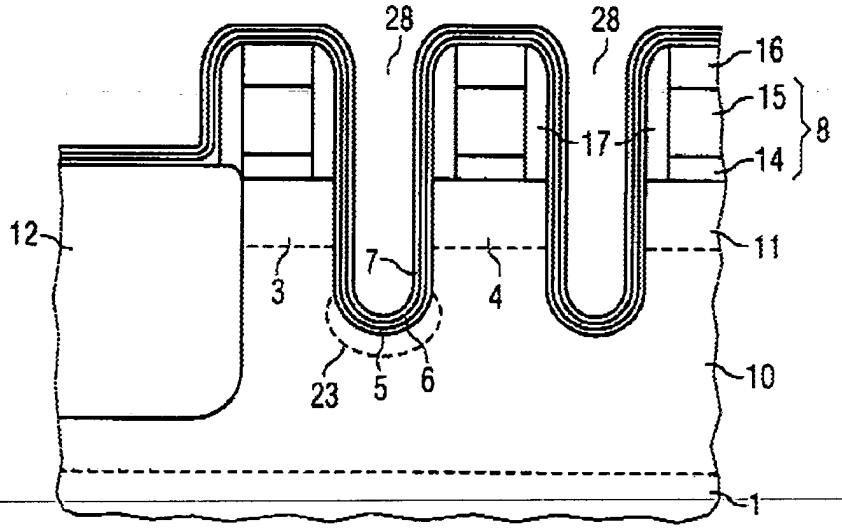


FIG 3



applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric (ONO layer) and including a lower boundary layer **5**, a storage layer **6**, and an upper boundary layer **7** (col. 6, lines 20-32 and FIG. 3);

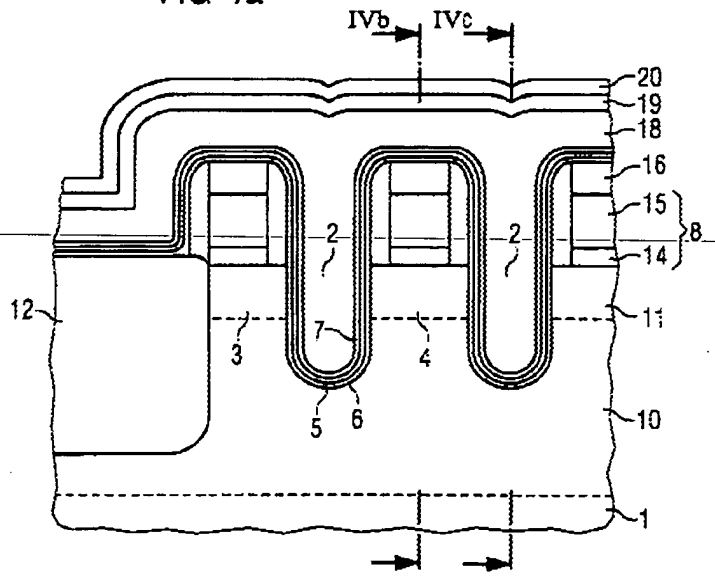
forming an oxide region in each case on a side of the doped regions remote from the semiconductor body , the oxide region being thicker than the lower boundary layer (col. 5, lines 8-46 and FIG. 3);

before the upper boundary layer is applied, and after the application of the storage layer, applying a sacrificial layer made from polysilicon and a material selectively etchable with respect to a material of the storage layer to the storage layer (col. 5, line 47 to col. 6, line 59);

producing openings **28** in the sacrificial layer, the storage layer, and the lower boundary layer, extending the semiconductor body **1**, by using a mask (col. 5, line 60 to col. 6, line 19);

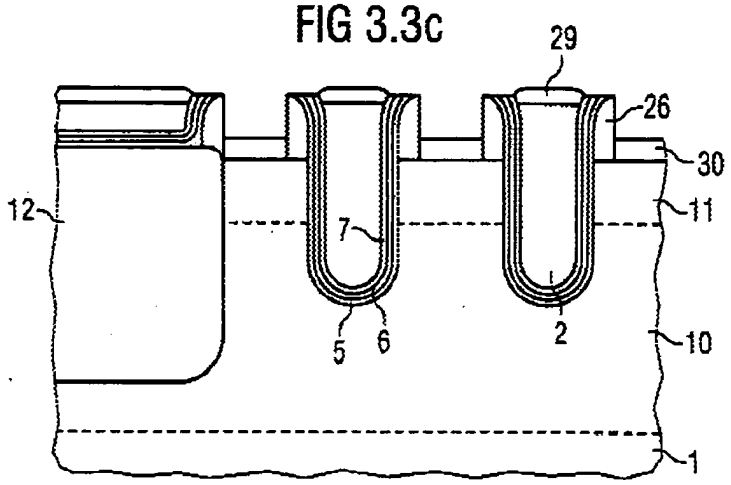
introducing doped polysilicon **18** into the openings (col. 6, lines 47-59 and FIG. 4a);.

FIG 4a



removing the sacrificial layer (col. 5, line 60 to col. 6, line 19); and producing the upper boundary layer **7** on the storage layer **6** and oxidizing at least a proportion of the polysilicon to form the oxide region **29** (col. 9, lines 9-46 and FIG. 3.3c).

FIG 3.3c



In re claim 2, **Palm** discloses that the sacrificial layer is produced as a deposited oxide (col. 5, line 60 to col. 6, line 19).

In re claim 3, **Palm** discloses that the method according claim 1 which further comprises selecting the storage layer from a group of materials consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide, zirconium oxide, aluminum oxide, and intrinsically conductive silicon (col. 3, lines 25-46).

In re claim 4, **Palm** discloses a method for fabricating a buried bit line for a semiconductor memory, which comprises: producing strip-like doped regions parallel to and at distances from one another in a semiconductor body **1**, the strip-like doped regions being adapted to act as bit lines and as source/drain regions **(3, 4)** of a respective memory transistor (col. 5, line 47 to col. 6, line 19 and FIGS. 2b-3);

applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric (ONO layer) and including a lower boundary layer **5**, a storage layer **6**, and an upper boundary layer **7** (col. 6, lines 20-32 and FIG. 3);

forming an oxide region in thicker than the lower boundary layer, in each case, on a side of the doped regions remote from the semiconductor body (col. 5, lines 8-46 and FIG. 3);

before producing the upper boundary layer, and after the application of the storage layer, applying a sacrificial layer with a topside to the storage layer (col. 5, line 47 to col. 6, line 59);

producing openings **28** with lateral walls in the sacrificial layer, the storage layer, and the lower boundary layer, by using a mask (col. 5, line 60 to col. 6, line 19);

introducing dopant into implantation regions of the semiconductor body through openings (col. 5, line 60 to col. 6, line 59 and FIG. 4a);

etching back the lateral walls of the openings and a topside of the sacrificial layer (col. 5, line 60 to col. 6, line 19) at an etching rate sufficient to form smooth sides on the sacrificial layer, the storage layer, and the lower boundary layer;

removing residues of the sacrificial layer selectively with respect to the storage layer (col. 5, line 60 to col. 6, line 19); and

producing the upper boundary layer **7** on the storage layer **6** and forming an oxide region **29** on a free surface of the semiconductor body, in each case between the sides (col. 9, lines 9-46 and FIG. 3.3c).

In re claim 5, **Palm** discloses that the method according to claim 4, which further comprises heating until the dopant introduce into the implantation regions has diffused to a portion of the semiconductor body covered by the storage layer (col. 9, lines 9-46).

In re claim 6, **Palm** discloses that the sacrificial layer is produced as a deposited oxide (col. 5, line 60 to col. 6, line 19).

In re claim 7, **Palm** discloses that the method according claim 4 which further comprises selecting the storage layer from a group of materials consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide, zirconium oxide, aluminum oxide, and intrinsically conductive silicon (col. 3, lines 25-46).

Response to Applicants' Amendment and Arguments

Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Applicants contend that the reference Park et al. (U.S. Patent 6,326,268), herein known as Park, do not disclose filling doped polysilicon into the openings of the layer sequence of the lower boundary layer, the storage layer, and the sacrificial layer, nor do Park et al. disclose the method by which the lateral walls of the openings are etched back to form smooth sides as shown in Fig. 8 of the instant application.

In response to applicants' contention that Park et al. do not disclose filling doped polysilicon into the openings of the layer sequence of the lower boundary layer, the storage layer, and the sacrificial layer, nor do Park et al. disclose the method by which the lateral walls of the openings are etched back to form smooth sides as shown in Fig. 8 of the instant application, Examiner respectfully disagrees. Since Applicants' amendment

necessitated the new ground(s) of rejection presented in this Office Action, the newly discovered reference, Palm et al. (U.S. Patent 6,548,861) teaches Applicants' claimed invention (See the rejection on pages 3-6 presented in this Office Action). Thus Applicants' argument is moot. For this reason, Examiner holds the rejection proper.

Conclusion

Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
December 14th, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER